



The Data system for the Next Generation Space Telescope (NGST) Integrated Science Module (ISM) is the primary data interface between the spacecraft, telescope, and science instrument systems. This poster includes block diagrams of the ISM data system and its components derived during the pre-phase A Yardstick feasibility study. The poster details the hardware and software components used to acquire and process science data for the Yardsick instrument complement, and depicts the baseline external interfaces to science instruments and other systems. This baseline data system is a fully redundant, high performance computing system. Each redundant computer contains three 150 MHz power PC processors. All processors execute a commercially available real time multi-tasking operating system supporting, preemptive multi-tasking, file management and network interfaces. These six processors in the system are networked together. The spacecraft interface baseline is an extension of the network, which links the six processors. The final selection for Processor busses, processor chips, network interfaces, and high-speed data interfaces will be made during mid 2002.

Software task diagrams with data flow paths are presented to summarize all aspects of the system. This software configures the instruments for an observing mode, using an event-based scheduler included in the ISIM Data system software. The software also operates custom Field Programmable Gate Array hardware to acquire and process the data from the three Yardsstick science instruments, which are operated independently. The software also operates hardware in the ISIM data processor to compress and format the science data into observation file records. These observation files are transferred to the spacecraft data system using a network interface. Non real time software in the ISIM data system computes primary mirror figure and focus commands required to tune the telescope for optimal performance. The ISIM data system software also delivers a real-time fine guidance command derived from processed wide field camera data.

The goal of the NGST ISIM data system pre-phase A activity was to determine whether development of a data system that meets the needs of NGST could be accomplished using the technology expected to be available in the NGST timeframe. Additionally, cost and performance trade studies were performed for FPA sizes from 50 to 400 mega-pixels with readout times of 2 to 15 seconds. Limiting areas were identified and characterized based FPA size and readout time. This work is valuable for future instrument and spacecraft trade studies to be executed during the NGST phase A.

NGST ISIM Data system requirements:

- Collect focal plane array data: 5 - 4096 X 4096 arrays and 1-1024X1024 array, 2-15 second readout times. Support ground communications- accept ground and S/C commands and files, send files to ground.
- Select and track guide star using a single 1024 X1024 detector in main array. Use guide star data to generate fast steering mirror commands and S/C centering control commands. 100 Hz control loop is required.
- Support off-line wave-front processing (mirror figure control) based on focal plane array data. Deformable mirror and Optical Telescope Assembly control commands.
- Provide on-board health and safety monitoring of spacecraft and instrument components.
- Provide "event driven" (adaptive) science scheduling capability.
- Provide instrument command and control capability.

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The diagram illustrates the architecture of the NGST Flight Data System, divided into three main functional areas: Spacecraft, ISM, and Host-side/Cold-side.

- Spacecraft:**
 - SC Data Handling & Control Systems:** This block contains a vertical stack of components: ADC, Attitude Control, Guidance, and Autopilot.
 - Primary & Secondary Mission Data:** This block includes a vertical stack: Mission Data, Data Distribution, and Data Collection.
 - Communications Subsystem:** This block includes a vertical stack: Communications, Data Link, and Antenna.
- ISM (Instrument Support Module):**
 - ISM Data Analysis Functions:** This block includes a vertical stack: Basic Data Analysis, Data Reduction, Data Archiving, and Data Distribution.
 - Mission Control Functions:** This block includes a vertical stack: Mission Planning, Mission Execution, and Mission Monitoring.
- Host-side / Cold-side:**
 - Host-side:** This block includes a vertical stack: Host Data, Host Control, and Host Monitoring.
 - Cold-side:** This block includes a vertical stack: Cold Data, Cold Control, and Cold Monitoring.

Arrows indicate the flow of data and control signals between these components, showing a complex interconnection between the spacecraft, the ISM, and the ground-based host/cold-side systems.

The diagram illustrates the Redundant Mechanism Control Bus architecture. It features two parallel processing paths, each consisting of an SSI Processor (A and B) connected to a Mechanism Controller (A and B). These controllers are linked to Mechanism Electronics (A and B), which in turn control the Mechanisms (A and B). The system is designed for redundancy, with components labeled as '1°C REDUNDANT'. A legend indicates that green boxes represent SSI Hardware, pink boxes represent Redundant VSW Warm, and blue boxes represent Mechanisms Cold.

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graph LR
    subgraph "1°C REDUNDANT"
        direction TB
        SSI_A[SSI PROCESSOR A] --- MC_A[Mechanism Controller Mechanism A]
        SSI_B[SSI PROCESSOR B] --- MC_B[Mechanism Controller Mechanism B]
        MC_A --- ME_A[Mechanism Electronics A]
        MC_B --- ME_B[Mechanism Electronics B]
        ME_A --- M_A[Mechanisms A]
        ME_B --- M_B[Mechanisms B]
        SSI_A --- SSI_B
        MC_A --- MC_B
        ME_A --- ME_B
        M_A --- M_B
    end
    style SSI_A fill:#90EE90
    style SSI_B fill:#90EE90
    style MC_A fill:#90EE90
    style MC_B fill:#90EE90
    style ME_A fill:#FFB6C1
    style ME_B fill:#FFB6C1
    style M_A fill:#ADD8E6
    style M_B fill:#ADD8E6

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Optimum mechanism control scheme drivers:

- Wire restrictions imposed by thermal isolation truss may require a compact instrument mechanism control bus
- Power restrictions for warm side electronics may not allow buses like MIL-STD-1553B to be used
- Power of bus interface chips is high (3-4 watts per interface)
- I Squared C may be a good compromise for a mechanism control bus
 - Minimizes impact on thermal truss wiring
 - Industry standard bus
 - Low cost GSE equipment available
 - Simple low power protocol
 - Speed up to 400 kbps
- Hardware / software development cost and simulator development will be a significant cost driver
- Industry standard bus highly desirable for cost reasons

Figure 1 is a block diagram titled "REDUNDANT MECHANISM CONTROL BUS". It illustrates a redundant control architecture. On the left, two "ISM PROCESSOR A" and "ISM PROCESSOR B" blocks (green) are connected to a central vertical "BUS" block (green). The "BUS" block is connected to two "MECHANISM CONTROLLER INSTRUMENT A" and "MECHANISM CONTROLLER INSTRUMENT B" blocks (yellow). These controllers are connected to "MECHANISM ELECTRONICS" blocks (pink), which in turn connect to "MECHANISM" blocks (blue). A legend at the bottom identifies the colors: green for ISM HARDWARE, yellow for INSTRUMENT HW FCT, pink for INSTRUMENT FW BARM, and blue for MECHANISM CONTROL.

- Use of flight hardware identical in function to commercially available hardware enables lower system development costs.
- Power PC architecture baseline because of X2000 power PC enables the use of commercial software development tools and commercial real time operating systems. Commercial software standards can also be used. Several commercial real time operating systems exist which support Internet protocols
- Commercial bus architectures will be used where practical to reduce cost and to allow the use of commercial designs and test equipment. Commercial communication interfaces will be used where practical to allow standard off the shelf hardware to be used in the system
- Simplifies interface testing by allowing use of commercial interface documentation, test sets, training, and hardware.

- Continue to investigate pixel processing algorithms
- Continue processor, data link and back-plane bus investigations.
- Investigate use of redundant processors for TIR and spectrometer to increase software costs
- Develop software integration and test methodologies, and assess hardware impacts
- Develop flight code development and test paradigms for use at instrument institutions and assess hardware, software and cost impacts.
- Should algorithms be implemented which exclude "statistically bad sample differences" from slope fit, but which includes these "bad" differences in the data stream to allow the ground to verify or reverse the correction process. (The Jurotchik/Knox method.)
- Will a full cosmic ray identification algorithm be implemented in the ISIM data system
- What forms of compression will be used in the NGST ISIM.
 - Need to perform study with actual/simulated NGST/HST data and flight algorithms currently implemented in flight qualified parts.
 - Currently 3.0 to 1.0 compression is baseline. A specific implementation for this compression must be defined during the pre-flight activities.
 - Current flight qualified compression chips operate at about 2:1 compression ratio
 - NGST compression should be executed in hardware because of high data rate
 - A cost trade including the cost of compression vs the ground flight test systems impacts must be performed during as part of the Phase A.
- Define ISIM data system architectures for large arrays at fast readout rates to enable the preparation of a cost model.

The diagram illustrates the data flow within the NGST Flight Data System, divided into three main functional areas: PCH Processing, UC Data Handling, and DBS Data Analysis.

- PCH Processing:** This section on the left handles incoming data from various sources including the PCH, PCH-1, PCH-2, and PCH-3. It also receives data from the PCH-4 and PCH-5. The data is processed through a series of steps: PCH Data Input, PCH Data Processing, PCH Data Output, and PCH Data Storage. The output of this section is then sent to the UC Data Handling section.
- UC Data Handling:** This central section manages the flow of data between the PCH Processing and DBS Data Analysis sections. It includes components for UC Data Input, UC Data Processing, UC Data Output, and UC Data Storage. The data is processed through a series of steps: UC Data Input, UC Data Processing, UC Data Output, and UC Data Storage. The output of this section is then sent to the DBS Data Analysis section.
- DBS Data Analysis:** This section on the right performs detailed analysis on the data received from the UC Data Handling section. It includes components for DBS Data Input, DBS Data Processing, DBS Data Output, and DBS Data Storage. The data is processed through a series of steps: DBS Data Input, DBS Data Processing, DBS Data Output, and DBS Data Storage. The output of this section is then sent to the DBS Data Storage section.

The diagram also shows a feedback loop from the DBS Data Storage section back to the UC Data Handling section, indicating that data is stored and then retrieved for further processing. Additionally, there is a direct path from the UC Data Handling section to the DBS Data Storage section, suggesting that data can be stored directly without intermediate processing.

- FPA processing can operate at full detector rate (ie no dead time)
- FPA processing has been partitioned between hardware state machines and software because of the high pixel counts
- End point averaging
 - N samples at start added to sum
 - N samples at end subtracted from sum
 - Final sum reported as result
- Slope fit
 - 16 samples or averages of samples, read at irregular intervals over 1000 seconds
 - Slope found using LMS line fit (derivation available)
 - Slope is computed not offset
 - Time of each sample or sample average is required
 - Value beyond linear range are not included in slope
- Both algorithms are implemented with helper hardware
- End point averaging or sample averaging uses a memory unit with add or subtract to location capability
- Slope fit is baseline for software but could be implemented in hardware which implements $z = s + x \cdot y$ (could be implemented in dsp)

RAW DATA

WEIGHTED COS SLOPE 1D FFT

SPECTRA

REGISTRATION PERIOD (PRT)

REGISTERED SPECTRA

COSINE WEIGHTING / BEST FREQUENCIES

SCIENCE DATA

- Irregular sampling in time domain reduces computational loading while increasing dynamic range
- Dynamic Range $[0, -\text{Gain} \cdot \text{Qin} \cdot \text{FULL_WELL}]$ or $(\text{DELAY} + \text{Dt})$
 - About 500 times greater dynamic range compared to one-point averaging
- Avg 2.4, 8, 16, 32 can be implemented in hardware at low cost
- Cosmic ray processing possible for time scales $> 32 \cdot \text{Dt}$
- Science data rate proportional to Dt/K
- Average computation requires $16W (\# \text{pixels} / \text{Dt})$ OPs
- SW slope flt $(10^4 \# \text{pixels}) / 32 \text{ HOPS}$

• Dynamic range $[0, \text{Gain} \times \text{Cie} \times \text{Full_well}] / \text{DT}$.

• Science data rate Proportional To Dt / K .

• Average computational requirements: $((2N+2) \times (\text{FrameRate}) \times \text{Idt})$ (no cosmic ray).

• Processing can be implemented in hardware at low cost for any possible array size.

• Science data is averaged over $\text{Dt} \times K$.

• Completely linear system with exception of optional cosmic ray software.

- Currently assuming 10% of all pixels will be impacted every 1000 seconds
- Detector parameters may change after impact.
- Recovery time is not currently modeled.
- Detecting some cosmic ray events is possible when in slope measurement state
 - Compute differences between slope samples.
 - Look for statistical abnormalities in ISM, (could be quite computationally intensive).
 - Could take transform of difference data to look for abnormal frequency content
 - Could compare pixel with adjacent pixels to look for statistically significant events (tremendous amount of on board processing)
- What should be done if abnormality is found.
 - Do nothing (less than 10 seconds). Clean data using ground processing (baseline)
 - Mark pixel as bad data
 - Exclude from slope algorithm bad differences and differences for TBD additional samples
 - Exclude from difference algorithm could be included in telemetry to allow bad data to be reconstructed during ground processing
 - Send all the samples for suspect pixels to the ground
 - generates more data (X 2.6)
- ISM required hardware must be customized for cosmic ray clearing algorithm
- Current baseline does not include computational overhead for cosmic ray clearing

- **ISIM Yardsstick Data System Impacts for Large FPA Arrays**
- Average Science data rate will increase proportional to FPA pixel count.
 - Higher down link rate. Ka band, higher power, or more ground stations
 - More compression: 3D lossless compression - No hardware available
- Data rate between FPA electronics and ISIM processor increases proportional to pixel count and inversely proportional to FPA readout time.
 - More fiber cable interfaces required.
 - Develop higher speed flight fiber interface for NGST, 10 Gbit/s available for ground use)
 - Higher processing power required
 - Use lower cost Digital Signal Processor to perform pixel processing
 - Lower cost if more than three Power PC processors are required
 - Fight against with commercial equal could be selected
- Compression becomes an issue because hardware lossless compression limited to 2 to 1.
 - Higher lossless compression rates will require pixel compression over time.
- Main bus of ISIM processor must provide sufficient bandwidth. Currently one main bus for each fiber optic FPA interface is required. Processors would be dedicated to certain sections of the FPA. Processors would communicate on a secondary bus like IEEE-1355.

The graph plots Data Rate (millions of bits per second) on the Y-axis (0 to 9) against Total Mega-pixels in Focal Plane Array (FPA) on the X-axis (0 to 400). Three studies are compared: SAMOS/TRACE, ESA, and UA STUDY. The UA STUDY shows the highest data rates, reaching 8 million bits per second at 400 mega-pixels. The SAMOS/TRACE and ESA studies show lower data rates, reaching approximately 3.5 million bits per second at 400 mega-pixels. The graph also includes horizontal lines indicating data rates for 3:1 compression and playback rates.

Total Mega-pixels in FPA	SAMOS/TRACE (Data Rate)	ESA (Data Rate)	UA STUDY (Data Rate)
50	1.0	1.0	1.0
100	1.5	1.5	1.5
150	2.0	2.0	2.0
200	2.5	2.5	2.5
250	3.0	3.0	3.0
300	3.5	3.5	3.5
350	3.5	3.5	3.5
400	3.5	3.5	8.0

Legend:

- ◼ GIM Science Data Rate
- ◼ After 3:1 compression
- ◼ Playback Rate

The graph plots Memory Size (Millions of Bytes) on the Y-axis (0 to 3000) against Mega pixels in Focal Plane Array (FPA) on the X-axis (50 to 400). Three data series are shown: YAG:STEC (red diamonds), ESA (blue squares), and UA STUDY (green triangles). The UA STUDY series shows a steep, linear increase in memory size as FPA resolution increases, while the YAG:STEC and ESA series remain relatively flat and low.

Mega pixels in FPA	YAG:STEC (MBytes)	ESA (MBytes)	UA STUDY (MBytes)
50	~100	~100	~400
100	~150	~150	~1000
150	~200	~200	~1600
200	~250	~250	~2200
250	~300	~300	~2800
300	~350	~350	~3400
350	~400	~400	~4000
400	~450	~450	~4600

Annotations on the graph:

- Vertical line at 100 Mega pixels: YAG:STEC
- Vertical line at 150 Mega pixels: ESA
- Vertical line at 350 Mega pixels: UA STUDY
- Text at top right: "Possible but will still drive cost and complexity need to switch memory technology" (pointing to the UA STUDY line)
- Text at top right: "Increase FPA data as it enables reducing memory requirement significantly" (pointing to the UA STUDY line)
- Text at bottom right: "Baseline" (pointing to the YAG:STEC and ESA lines)
- Text at bottom right: "Cost will still be reduced by processing chips as they arrive" (pointing to the YAG:STEC and ESA lines)

Total Mega-pixels in FPA	2 sec FPA readout (billions bits/sec)	1 sec FPA readout (billions bits/sec)	1/2 sec FPA readout (billions bits/sec)
50	~500	~300	~200
100	~600	~400	~250
200	~800	~550	~300
300	~1100	~700	~350
400	~1400	~850	~400

Figure 10 is a line graph titled "Performance of the proposed architecture". The Y-axis is labeled "Millions of Operations per second" and ranges from 0 to 250. The X-axis is labeled "Total Mega-pixels in Focal Plane Array (PA)" and ranges from 50 to 400. There are three data series: "End Point MOPS (MOPS)" represented by blue diamonds, "Slope FP MOPS (MOPS)" represented by purple squares, and "Slope FIT MOPS (MOPS)" represented by green triangles. Two horizontal lines indicate performance levels: a green line at 150 MOPS labeled "Performance Level of 150 MOPS (green)" and a purple line at 210 MOPS labeled "Performance Level of 210 MOPS (purple)". The End Point MOPS series starts at approximately 100 MOPS for 50 MPa and reaches 200 MOPS for 400 MPa. The Slope FP MOPS series starts at approximately 50 MOPS for 50 MPa and reaches approximately 150 MOPS for 400 MPa. The Slope FIT MOPS series starts at approximately 20 MOPS for 50 MPa and reaches approximately 100 MOPS for 400 MPa.

Total Mega-pixels in Focal Plane Array (PA)	End Point MOPS (MOPS)	Slope FP MOPS (MOPS)	Slope FIT MOPS (MOPS)
50	100	50	20
100	120	70	30
150	140	90	40
200	160	110	50
250	180	130	60
300	200	140	70
350	210	150	80
400	220	150	100